OPEN TO SELECT OPPORTUNITIES

JOSH HUANG 黃致學

PRINCIPAL DIGITAL IC DESIGNER | AI-NATIVE RTL WORKFLOW PIONEER

Taipei City, Taiwan jamphus@gmail.com +1-425-998-6872 linkedin.com/in/huangjs

DOC NO.	REVISION	EXPERIENCE	STATUS
JCH-RESUME-03	2026.07	18+ years	Active

01 GENERAL DESCRIPTION

CS-educated (**NCTU / NTHU**) digital IC designer with **18+ years** of high-performance silicon design across MStar, Ubiquiti, Bitmain/Cvitek and ASPEED. Specializes in **“software-defined hardware design”** — using a computer-science background to re-architect traditional EDA environments rather than operate inside their defaults.

Currently a high-intensity **ChipAgents power user**, having built a proprietary methodology for the “last mile” of AI in RTL design: agentic close-loop systems for autonomous testing, real-time error correction, and full-stack architecture standardization.

Earlier chapters span ISP system architecture for silicon that shipped as BM1880V2 / CV1835 / CV1820, RTL for Ubiquiti’s airFiber LTU and GPON OLT product lines, and 34+ taped-out chips at MStar across 2G basebands, video codecs and touch/display IP.

02 FEATURES

DIGITAL IC DESIGN & LEADERSHIP

High-speed RTL (Verilog/SystemVerilog), ISP 3A/HDR/CFC, BMC architecture, timing closure, power/area optimization, CDC, formal verification, automated ECO, CPF low-power flow.

AGENTIC MASTERY

“Divide-and-conquer” agent guiding, real-time agent pivoting, context/memory management for complex RTL generation via ChipAgents.

AUTOMATION & INFRASTRUCTURE

Python (FastAPI/CLI), C/C++ (DPI-C), Perl, Tcl/Tk, Jenkins CI/CD (22+ jobs), Docker, QEMU, SVN/Git/P4.

EDA FLOW INNOVATION

Full-stack unified design environments (C-model to firmware), bit-true co-simulation, Cadence Conformal LEC, VMM/UVM verification IP, automated regression.

03 APPLICATIONS — EXPERIENCE

JUN 2022
— PRESENT

CURRENT

Principal Digital IC Designer & Design Efficiency Lead

ASPEED Technology · Taipei, Taiwan

- De facto end-to-end owner of the ISP subsystem — RTL through Conformal LEC sign-off and GUC foundry-deliverable packaging — with **~15,300 authored commits across 5 product repositories** over 4 years (**10× the next-highest contributor** on the primary IP repo) and a 103-file reusable common IP library used across ~80 ISP unit blocks.
- Closed hierarchical Conformal LEC on a large frozen netlist to **0 NEQ with 0 manual pin-constraints** — a chip-blocking equivalence problem no other engineer had cleared — delivering the FULL-EQ verdict directly to chiptop owners with the final netlist md5-verified before sign-off.
- Audited handshake modules against the ARM AMBA AXI-Stream specification, identified a real deadlock condition, and shipped a spec-compliant replacement with a written compliance proof.
- Owned the GUC foundry-deliverable interface end-to-end — UNS screening driven to a clean pass, SRAM-compiler upgrade fallout resolved, packaging automation built, and a daily automated status report so hand-offs never silently stalled.
- Directed ChipAgents through 20+ iterative modifications to architect a production-grade ISP Auto Focus module — 100% coding-style compliance and timing closure inside an autonomous, close-loop environment.
- Architected a full-stack unified IP flow (C-model → firmware) across **103 IP modules**: design, synthesis, lint, LEC, ECO and firmware-header generation with zero-manual-intervention handoffs across the HW/SW boundary.
- Built an autonomous ISP bit-true co-simulation framework (DPI-C) for 6+ core ISP modules, debugging EOF/EOL pipeline-sync issues to 100% bit-true alignment.
- Re-engineered SmartSramGen from a simple Q&A model into a ChipAgents-driven autonomous system self-correcting across 600+ instances.
- Developed a “strategic guiding” methodology that overcame agentic-adoption friction for senior engineers reverting to legacy flows — internal champion for AI-native workflows.

- Optimized 22 Jenkins pipeline jobs and used AI for knowledge management, cutting RTL team onboarding time.

JUL 2018 — JUN 2022

Lead ISP Digital Designer

Bitmain / Cvitek · Taipei, Taiwan

- Major contributor to ISP designs across Bitmain / ICLink / Wisecore / Cvitek — AE, HIST, AF, AWB, GMS, LSCM, DCI, LDCI, FPN, BLC, WBG.
- IP shipped in every chip taped out on the line: BM1880V2, CV1835, CV1820 — top subsystem integration, IP and system verification.
- Built and maintained the ISP IP verification environment; developed the ISP system addressing automation flow.
- Owned the Jenkins-CI regression flow; built ISP C-model co-simulation and integration with RTL.
- Architected IP block structure and translation from C-model; drove IP cost-down and power-saving.

DEC 2013 — JUN 2018

SoC Design Engineer

Ubiquiti Networks · Taipei, Taiwan

- Designed RTL blocks for shipping communications products — airFiber LTU (FFT/iFFT engines, batch programmer engine, DFS engine, memory wrappers) and GPON OLT, in Verilog/SystemVerilog.
- Integrated million-gate 28nm ASICs through synthesis, CDC, formal verification, automated ECO, and power & timing closure.
- Brought up airFiber LTE in the field and debugged post-silicon CPU/bus issues.
- Ran block- and chip-level verification on FPGA (Altera and Xilinx); developed the automated ECO flow for Conformal ECO.
- Introduced elegant SystemVerilog methods — interfaces, parameterization, assertions — and a Jenkins-CI regression system.
- Developed ARM-DSM simulations, a NAND controller, an LVDS companion-RF interface, and a U-Boot driver for Altera's low-latency 10GbE MAC/PHY.
- Worked daily across sites in America, Europe and Asia.

APR 2008
— DEC 2013

Senior Digital IC Designer & Automation Lead

MStar Semiconductor (acquired by MediaTek) · Hsinchu, Taiwan

- Owned RTL design SPEC-to-tapeout for touch screen, 2G digital baseband, video codec (AVC/H.264, RMVB, VP6, HEVC/H.265), AMBA/bus-protocol translation, memory BIST/scan-ATPG (DFT), power-aware gating and SIM-card IP.
- Built VMM/UVM SystemVerilog verification environments and a reusable OCP verification IP.
- Ran ARM/DSP-based design and simulation with C-code co-simulation.
- Generated RTL via Perl/TCL; built “dropzone,” an automated regression system in Python/Perl/crontab.
- Participated in **34+ taped-out chips** — A/D TV, 2G/3G handset, set-top box and GPS — from .18μm down to 28nm.
- Equipment-level debug with oscilloscope, JTAG ICE, logic analyzer and Keithley source meters.

Early career — StarVedia Technologies, part-time software engineer, 2006–2007 (C#/C++ surveillance-system GUI); freelance contract, 2005 (RSS aggregator: PHP/CSS front-end, Java/MySQL back-end).

04 EDUCATION

2005
– 2007

National Tsing Hua University

M.S., Computer & Information Science

Thesis: “Design and Implementation of Gradient Domain Compression and Photographic Tone Mapping for Real-Time High Dynamic Range Video”

2001
– 2005

National Chiao Tung University

B.S., Computer & Information Science

05 NOTES — HONORS & CERTIFICATES

2013.07	TOEIC — scored 905/990. “Ability to communicate effectively in almost any situation.”
2012	MStar Semiconductor Short-Term Reward Winner
2011	MStar Semiconductor Short-Term Reward Winner
2013	Google Code Jam — Qualification Round passed
2006.05	GEPT (General English Proficiency Test) — High-Intermediate level
2005	Trend Micro Programming Contest — network monitoring system, C/C++

HJS.SPACE · JAMPHUS@GMAIL.COM